GIGALIGHT CXP-CXP Active Optical Cable
GCX-DO151G-XXXC

Features

- Full duplex 12 channel 850nm parallel active optical cable
- Transmission data rate up to 12.5Gbit/s per channel
- Hot pluggable electrical interface
- Differential AC-coupled high speed data interface
- 12 channels 850nm VCSEL array
- 12 channels PIN photo detector array
- Multi-mode optical fibre cable of up to 100m
- Management Interface and digital diagnostic monitoring through I2C
- Low power consumption
- Housing isolated from connector ground
- Operating case temperature 0°C to +70°C
- 3.3V power supply voltage
- RoHS 6 compliant

Applications

- 12.5Gbps Proprietary Interconnects
- Infiniband transmission at 12ch SDR, DDR and QDR
- Switches, Routers
- Data Centers

Description

CXP-CXP active optic cables are a high performance, low power consumption, long reach interconnect solution supporting 12.5G per channel Proprietary Interconnects,120G Ethernet, fiber channel and PCIe. It is compliant with the 120Gbits Small Form factor Hot-Pluggable CXP-interface. Gigalight CXP AOC is an assembly of 12 full-duplex lanes, where each lane is capable of transmitting data at rates up to 12.5Gb/s, providing an aggregated rate of 150Gb/s.

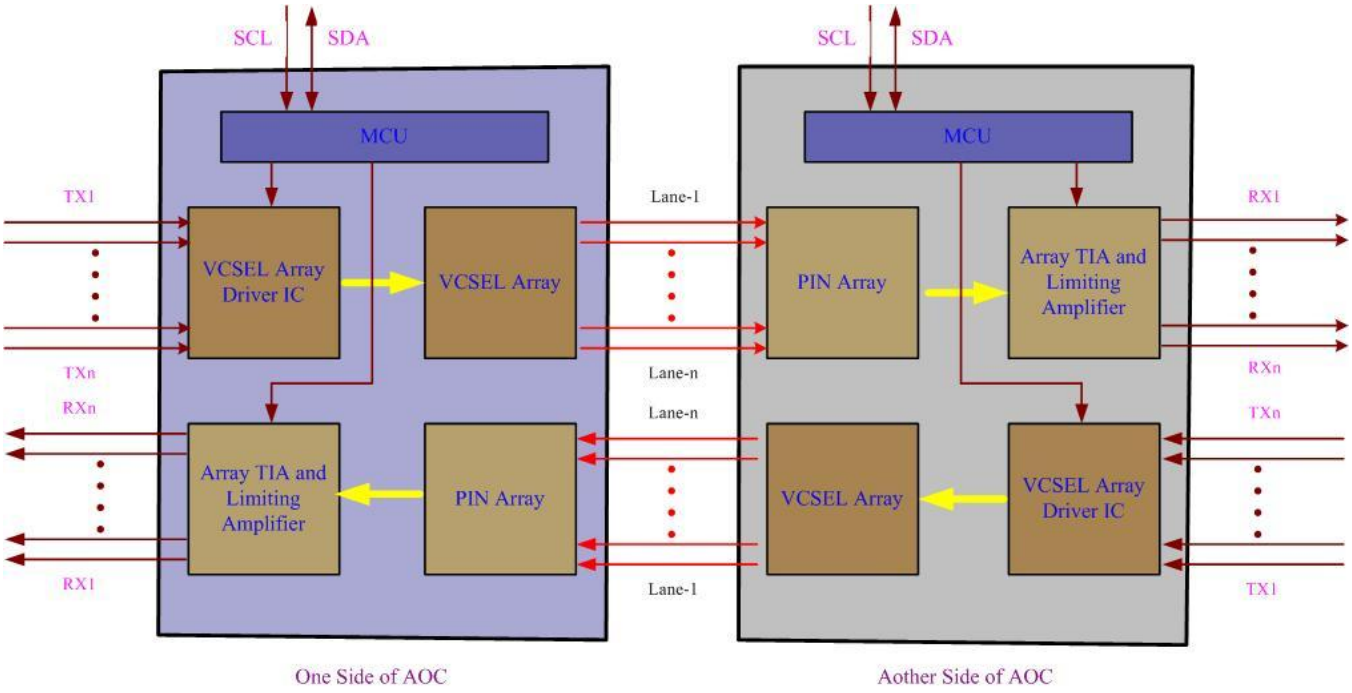


Figure1. Module Block Diagram

AOC is one kind of parallel transceiver. VCSEL and PIN array package is key technique, through I2C system can contact with module.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-20	85	ºC
Case Operating Temperature	Top	0	70	ºC
Humidity(non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case temperature	Tca	0		70	ºC
Data Rate Per Lane	fd			12.5	Gbps
Humidity	Rh	5		85	%
Power Dissipation	Pm			4	W
Fiber Bend Radius	Rb	3			cm

Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential input impedance	Zin	90	100	110	ohm
Differential Output impedance	Zout	90	100	110	ohm
Differential input voltage amplitude	ΔVin	200		1200	mVp-p
Differential output voltage amplitude	ΔVout	600		800	mVp-p
Skew	Sw			300	ps
Bit Error Rate	BR			E-12	
Input Logic Level High	VIH	2.0		VCC	V
Input Logic Level Low	VIL	0		0.8	V
Output Logic Level High	VOH	VCC-0.5		VCC	V
Output Logic Level Low	VOL	0		0.4	V

Note:

1. BER=10^-12; PRBS 2^31-1@10.3125Gbps.
2. Differential input voltage amplitude is measured between TxNp and TxNn.
3. Differential output voltage amplitude is measured between RxNp and RxNn.

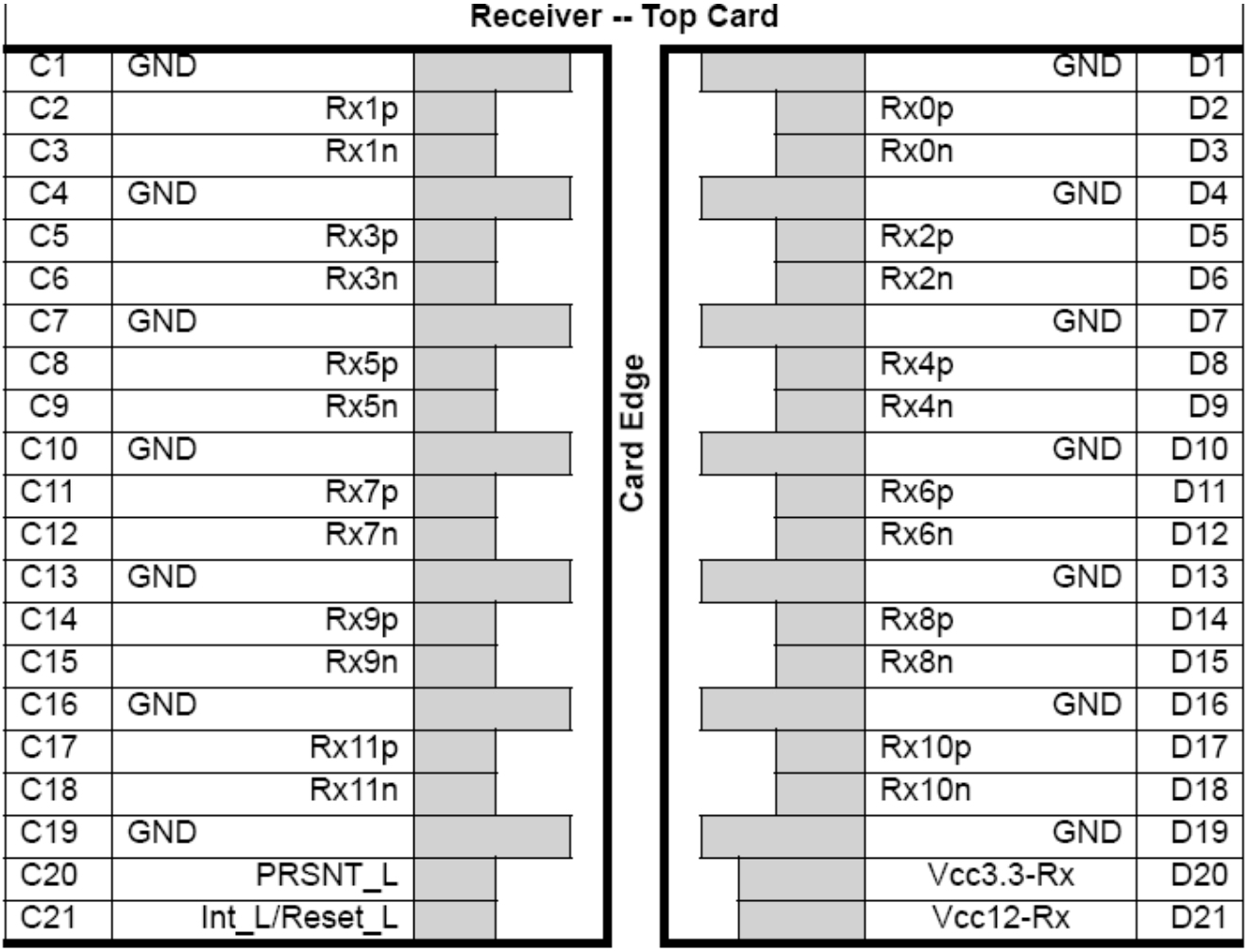
Pin Descriptions

Pin	Logic	Symbol	Name/Description	Ref.
A1		GND	Module Ground	1
A2	CML-I	Tx1+	Transmitter non-inverted data input	
A3	CML-I	Tx1-	Transmitter inverted data input	
A4		GND	Module Ground	1
A5	CML-I	Tx3+	Transmitter non-inverted data input	
A6	CML-I	Tx3-	Transmitter inverted data input	
A7		GND	Module Ground	1
A8	CML-I	Tx5+	Transmitter non-inverted data input	
A9	CML-I	Tx5-	Transmitter inverted data input	
A10		GND	Module Ground	1
A11	CML-I	Tx7+	Transmitter non-inverted data input	
A12	CML-I	Tx7-	Transmitter inverted data input	
A13		GND	Module Ground	1
A14	CML-I	Tx9+	Transmitter non-inverted data input	
A15	CML-I	Tx9-	Transmitter inverted data input	
A16		GND	Module Ground	1
A17	CML-I	Tx11+	Transmitter non-inverted data input	
A18	CML-I	Tx11-	Transmitter inverted data input	
A19		GND	Module Ground	1
A20	LVCMOS-I	SCL	2-wire Serial interface clock	2
A21	LVCMOS-I/O	SDA	2-wire Serial interface data	2
B1		GND	Module Ground	1
B2	CML-I	Tx0+	Transmitter non-inverted data input	
B3	CML-I	Tx0-	Transmitter inverted data input	
B4		GND	Module Ground	1
B5	CML-I	Tx2+	Transmitter non-inverted data input	
B6	CML-I	Tx2-	Transmitter inverted data input	
B7		GND	Module Ground	1
B8	CML-I	Tx4+	Transmitter non-inverted data input	
B9	CML-I	Tx4-	Transmitter inverted data input	
B10		GND	Module Ground	1
B11	CML-I	Tx6+	Transmitter non-inverted data input	
B12	CML-I	Tx6-	Transmitter inverted data input	
B13		GND	Module Ground	1
B14	CML-I	Tx8+	Transmitter non-inverted data input	
B15	CML-I	Tx8-	Transmitter inverted data input	

B16		GND	Module Ground	1
B17	CML-I	Tx10+	Transmitter non-inverted data input	1
B18	CML-I	Tx10-	Transmitter inverted data input	
B19		GND	Module Ground	1
B20		VCC3.3-TX	+3.3v Transmitter Power Supply	
B21		VCC12-TX	+12v Transmitter Power Supply, Unconnected	
C1		GND	Module Ground	1
C2	CML-O	RX1+	Receiver non-inverted data output	
C3	CML-O	RX1-	Receiver inverted data output	
C4		GND	Module Ground	1
C5	CML-O	RX3+	Receiver non-inverted data output	
C6	CML-O	RX3-	Receiver inverted data output	
C7		GND	Module Ground	1
C8	CML-O	RX5+	Receiver non-inverted data output	
C9	CML-O	RX5-	Receiver inverted data output	
C10		GND	Module Ground	1
C11	CML-O	RX7+	Receiver non-inverted data output	
C12	CML-O	RX7-	Receiver inverted data output	
C13		GND	Module Ground	1
C14	CML-O	RX9+	Receiver non-inverted data output	
C15	CML-O	RX9-	Receiver inverted data output	
C16		GND	Module Ground	1
C17	CML-O	RX11+	Receiver non-inverted data output	
C18	CML-O	RX11-	Receiver inverted data output	
C19		GND	Module Ground	1
C20	LVTTL-O	PRSNT_L	Module Present, pulled down to GND	
C21	LVTTL-I/O	INT_L/Reset_L	Interrupt output, Module Reset	2
D1		GND	Module Ground	1
D2	CML-O	RX0+	Receiver non-inverted data output	
D3	CML-O	RX0-	Receiver inverted data output	
D4		GND	Module Ground	1
D5	CML-O	RX2+	Receiver non-inverted data output	
D6	CML-O	RX2-	Receiver inverted data output	
D7		GND	Module Ground	1
D8	CML-O	RX4+	Receiver non-inverted data output	
D9	CML-O	RX4-	Receiver inverted data output	
D10		GND	Module Ground	1
D11	CML-O	RX6+	Receiver non-inverted data output	

D12	CML-O	RX6-	Receiver inverted data output	
D13		GND	Module Ground	1
D14	CML-O	RX8+	Receiver non-inverted data output	
D15	CML-O	RX8-	Receiver inverted data output	
D16		GND	Module Ground	1
D17	CML-O	RX10+	Receiver non-inverted data output	
D18	CML-O	RX10-	Receiver inverted data output	
D19		GND	Module Ground	1
D20		VCC3.3-RX	+3.3v Receiver Power Supply	
D21		VCC12-RX	+12v Receiver Power Supply, Unconnected	

Notes:
1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector; should be pulled up with 4.7k – 10k ohms on host board to a voltage between 3.15Vand 3.6V.



Transmitter -- Bottom Card

A1	GND			GND	B1
A2	Tx1p			Tx0p	B2
A3	Tx1n			Tx0n	B3
A4	GND			GND	B4
A5	Tx3p			Tx2p	B5
A6	Tx3n			Tx2n	B6
A7	GND			GND	B7
A8	Tx5p			Tx4p	B8
A9	Tx5n			Tx4n	B9
A10	GND			GND	B10
A11	Tx7p			Tx6p	B11
A12	Tx7n			Tx6n	B12
A13	GND			GND	B13
A14	Tx9p			Tx8p	B14
A15	Tx9n			Tx8n	B15
A16	GND			GND	B16
A17	Tx11p			Tx10p	B17
A18	Tx11n			Tx10n	B18
A19	GND			GND	B19
A20	SCL			Vcc3.3-Tx	B20
A21	SDA			Vcc12-Tx	B21

Card Edge

Figure2. Electrical Pin-out Details

PRSNT_L Pin： PRSNT_L is used to indicate when the module is plugged into the host receptacle. It is pulled down to GND through 5.2 kOhm in modules requiring 12V power, and tied directly down to GND in modules requiring 3.3V power only. Gigalight CXP Prsnt_L Pin internal directly connected to GND and just need single +3.3V Power Supply. The PRSNT_L signal is asserted “Low” when inserted and deasserted “High” when the module is physically absent from the host connector.

Int_L/Reset_L Pin： Int_L/Reset_L is a bidirectional signal. When driven from the host, it operates logically as a Reset signal. When driven from the module, it operates logically as an Interrupt signal. In both cases, the signal is asserted low, as indicated by the ’_L’ suffix. The Int_L/Reset_L signal requires open collector outputs in both the host and module, and must be pulled up on the host board. Int_L and Reset_L indications are

distinguished from each other by timing - a shorter assertion, driven by the module, indicates an interrupt, and a longer assertion of the signal, driven by the host, indicates a reset.

Int_L operation: When Int_L/Reset_L is pulled "Low" by the module for longer than the minimum interrupt pulse width (tInt_L,PW-min) and shorter than the maximum interrupt pulse width (tInt_L,PW-max) the signal signifies an interrupt. An interrupt indicates a possible module operational fault or a module status critical to the host system. The host identifies the cause of the interrupt using the 2-wire serial interface. Int_L must operate in pulse mode (vs. static mode), in order to distinguish a short interrupt signal from a longer reset signal, so the module must de-assert Int_L/Reset_L after the interrupt has been signaled.

Power Supply Filtering

The host board should use the power supply filtering shown in Figure3.

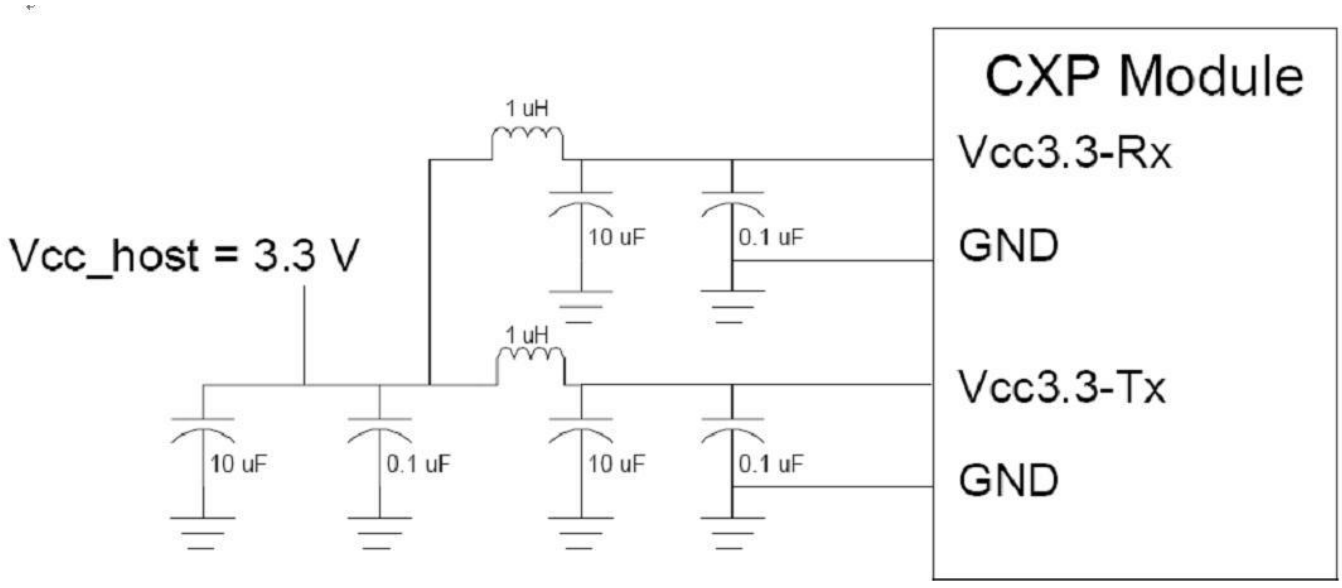


Figure3. Host Board Power Supply Filtering

DIAGNOSTIC MONITORING INTERFACE

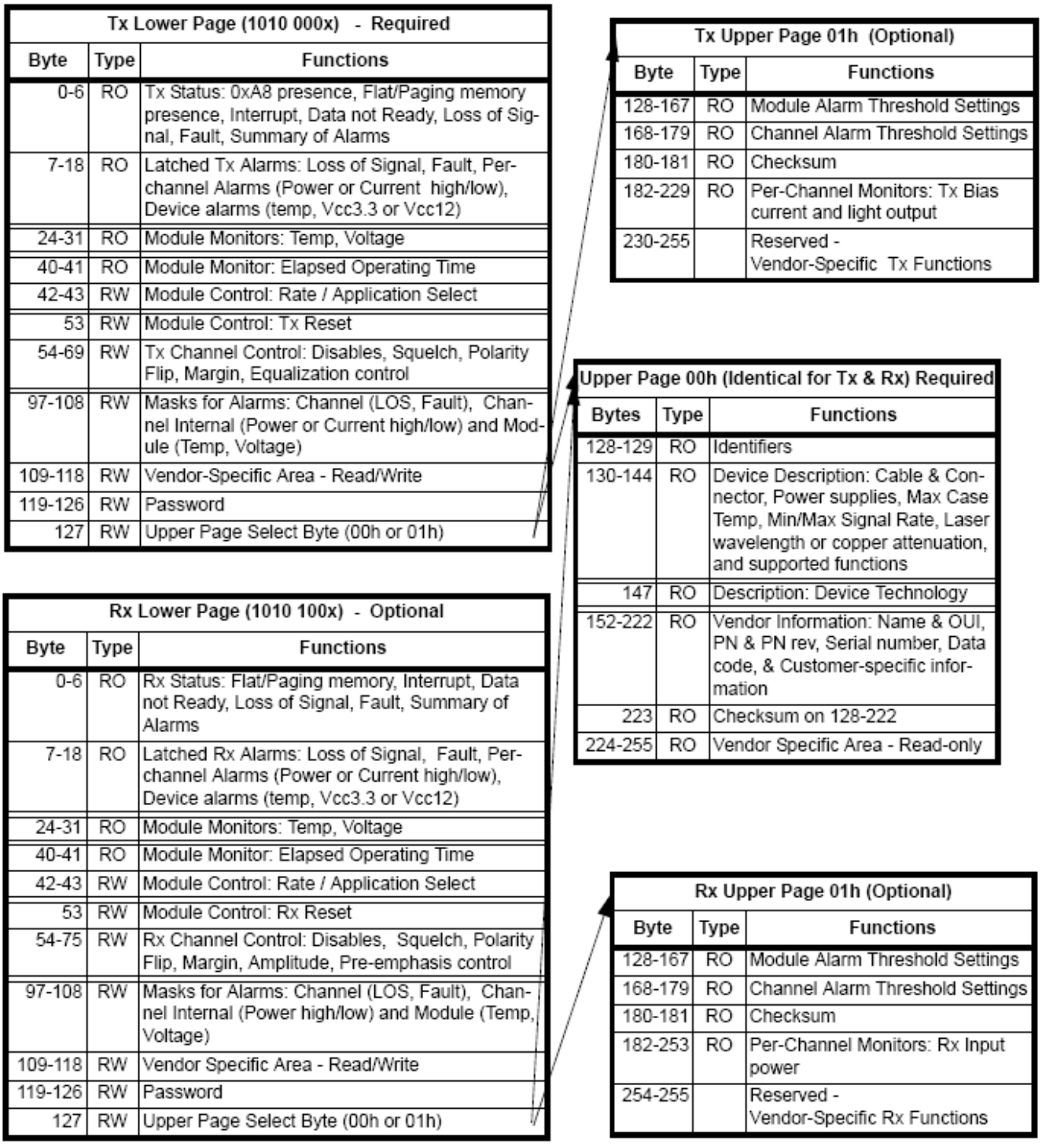
Digital diagnostics monitoring function is available on all Gigalight CXP AOCs. A 2-wire serial interface provides user to contact with module.

Figure 4 defines the Memory Map for CXP transceiver used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all CXP devices. The interface has been designed largely after the XFP MSA as defined in INF-8077i Rev.4.0. The memory map has been modified to accommodate 12 lanes per direction and to limit the required memory space. Paging on upper pages is used to allow slower access to less time-critical information.

The memory map has also been configured to support a range of device types, from simple passive cables with only EEPROM chips with two-wire serial interfaces for identification, to, for example, optical transceivers with tunable equalization and per-lane optical power monitoring. All devices conforming to this interface are required to implement a basic memory map, including various fields such as fields to identify the device type and manufacturer.

The structure of the memory map is shown in Figure 4 of next page. It includes two ranges of serial addresses, at 0xA0 (for Tx and basic required functions), and 0xA8 (for optional extensions, including Rx functions). Each address (0xA0 and 0xA8) contains one lower page and at least one upper page (00h), with one optional other upper page (01h) per address range. Each page contains 128 bytes of address space. The lower page or pages contain Read-Only information, and may contain Read-Write fields as well, for more sophisticated devices. The upper pages contain only Read-Only (RO) information. Only the first upper page (00h) is required. Other(s) are optional, to allow devices without pageable memory.

This structure permits timely access to fields in the lower page, which contain time-critical information, such interrupt flags, alarms, critical monitors (temperature, voltage,...) and per-lane control. Read-only device information such as serial ID information, vendor information, is available in Upper Page 00, which is identical for both 0xA0 and 0xA8 device addresses. Less time-critical Read-Only information on more complex devices, such as threshold settings or per-channel monitors, are available with the optional Upper Page Select function.



Tx Lower Page (1010 000x) - Required		
Byte	Type	Functions
0-6	RO	Tx Status: 0xA8 presence, Flat/Paging memory presence, Interrupt, Data not Ready, Loss of Signal, Fault, Summary of Alarms
7-18	RO	Latched Tx Alarms: Loss of Signal, Fault, Per-channel Alarms (Power or Current high/low), Device alarms (temp, Vcc3.3 or Vcc12)
24-31	RO	Module Monitors: Temp, Voltage
40-41	RO	Module Monitor: Elapsed Operating Time
42-43	RW	Module Control: Rate / Application Select
53	RW	Module Control: Tx Reset
54-69	RW	Tx Channel Control: Disables, Squelch, Polarity Flip, Margin, Equalization control
97-108	RW	Masks for Alarms: Channel (LOS, Fault), Channel Internal (Power or Current high/low) and Module (Temp, Voltage)
109-118	RW	Vendor-Specific Area - Read/Write
119-126	RW	Password
127	RW	Upper Page Select Byte (00h or 01h)

Tx Upper Page 01h (Optional)		
Byte	Type	Functions
128-167	RO	Module Alarm Threshold Settings
168-179	RO	Channel Alarm Threshold Settings
180-181	RO	Checksum
182-229	RO	Per-Channel Monitors: Tx Bias current and light output
230-255		Reserved - Vendor-Specific Tx Functions

Upper Page 00h (Identical for Tx & Rx) Required		
Bytes	Type	Functions
128-129	RO	Identifiers
130-144	RO	Device Description: Cable & Connector, Power supplies, Max Case Temp, Min/Max Signal Rate, Laser wavelength or copper attenuation, and supported functions
147	RO	Description: Device Technology
152-222	RO	Vendor Information: Name & OUI, PN & PN rev, Serial number, Data code, & Customer-specific information
223	RO	Checksum on 128-222
224-255	RO	Vendor Specific Area - Read-only

Rx Lower Page (1010 100x) - Optional		
Byte	Type	Functions
0-6	RO	Rx Status: Flat/Paging memory, Interrupt, Data not Ready, Loss of Signal, Fault, Summary of Alarms
7-18	RO	Latched Rx Alarms: Loss of Signal, Fault, Per-channel Alarms (Power or Current high/low), Device alarms (temp, Vcc3.3 or Vcc12)
24-31	RO	Module Monitors: Temp, Voltage
40-41	RO	Module Monitor: Elapsed Operating Time
42-43	RW	Module Control: Rate / Application Select
53	RW	Module Control: Rx Reset
54-75	RW	Rx Channel Control: Disables, Squelch, Polarity Flip, Margin, Amplitude, Pre-emphasis control
97-108	RW	Masks for Alarms: Channel (LOS, Fault), Channel Internal (Power high/low) and Module (Temp, Voltage)
109-118	RW	Vendor Specific Area - Read/Write
119-126	RW	Password
127	RW	Upper Page Select Byte (00h or 01h)

Rx Upper Page 01h (Optional)		
Byte	Type	Functions
128-167	RO	Module Alarm Threshold Settings
168-179	RO	Channel Alarm Threshold Settings
180-181	RO	Checksum
182-253	RO	Per-Channel Monitors: Rx Input power
254-255		Reserved - Vendor-Specific Rx Functions

Figure4. CXP Memory Map

The detail description of low memory and upper memory please see 120Gbit/s Small Form-factor Hot-Pluggable CXP-interface specification document.

Timing for Soft Control and Status Functions

Parameter	Symbol	Max	Unit	Conditions
Initialization Time	t_init	2000	ms	Time from power on[1], hot plug or rising edge of Reset until the module is fully functional[2]
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on[1] until module responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data	2000	ms	Time from power on[1] to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
Reset Assert Time	t_reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional[2]
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL = Vol
IntL Deassert Time	toff_IntL	500	μs	Time from clear on read[3] operation of associated flag until Vout:IntL = Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Interrupt Pulse Max Width	tintL,PW-max	50	μs	Max Time from falling edge of int_L pin output to rising edge of int_L pin output
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set and IntL asserted
Tx Fault Assert Time	ton_Txfault	200	ms	Time from Tx Fault state to Tx Fault bit set and IntL asserted
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted
Mask Assert Time	ton_mask	100	ms	Time from mask bit set[4] until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask	100	ms	Time from mask bit cleared[4] until associated IntlL operation resumes
Power_over-ride or Power-set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set [4] until module power consumption enters lower Power Level
Power_over-ride or Power-set Deassert Time	toff_Pdown	300	ms	Time from P_Down bit cleared[4] until the module is fully functional3
Parameter	**Symbol**	**Min**	**Unit**	**Conditions**

Interrupt Pulse Min Width	tintL,PW-min	5	μs	Min Time from falling edge of int_L pin output to rising edge of int_L pin output
Reset Pulse Min Width	Trst,PW-min	25	ms	Min Time from falling edge of Reset pin input to rising edge of Reset pin input

Note：

1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value.
2. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 deasserted.
3. Measured from falling clock edge after stop bit of read transaction.
4. Measured from falling clock edge after stop bit of write transaction.

Figure5. Timing Specifications

Mechanical Dimensions

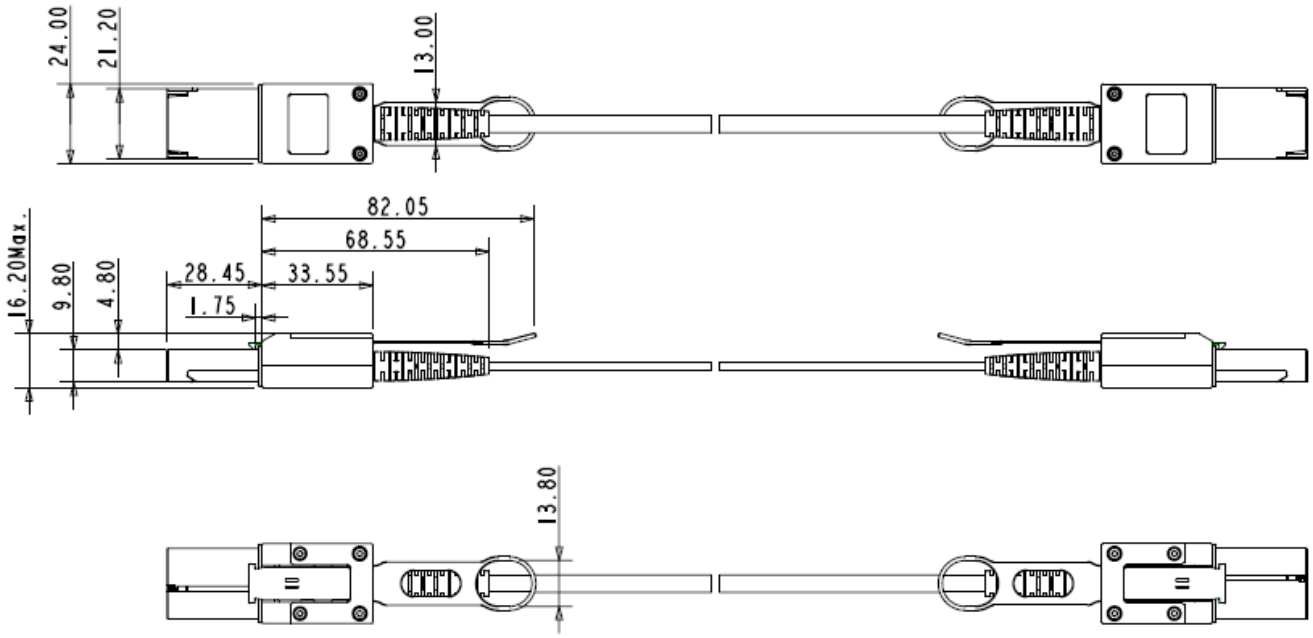


Figure6. Mechanical Specifications

Ordering information

Part Number	Product Description
GCX-DO151G-XXXC	**XXX**=different cable lengths

XXX	Cable Length

003	**003**=3m
005	**005**=5m
010	**010**=10m
020	**020**=20m
050	**050**=50m
100	**100**=100m

References

120Gbit/s Small Form-factor Hot-Pluggable CXP-interface

Important Notice

Performance figures, data and any illustrative material provided in this data sheet are typical and must be specifically confirmed in writing by GIGALIGHT before they become applicable to any particular order or contract. In accordance with the GIGALIGHT policy of continuous improvement specifications may change without notice.

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